Soft Breakdown and Hot Carrier Reliability of CMOS RF Mixer and Redesign

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Abstract **In this paper, CMOS RF down-conversion mixer circuit hot-carrier (HC) and soft breakdown (SBD) reliability estimation and redesign is presented. First of all, MOS transistor reliability under analog operation was evaluated by experiment. The mixer circuit operation conditions for the occurrence of HC and SBD are analyzed, and circuit performance model are presented to relate the device degradation to circuit performance degradation. Finally, we propose mixer circuit redesign strategies, which reduce the HC and SBD problem. Simulation shows improved noise performance with the similar gain, IIP3 and power consumption.**

I. INTRODUCTION

CMOS Gilbert cell down conversion mixer is a combination of high-speed digital circuit and high frequency RF circuit. Its current steering stages are high-speed switches. They are turn on and off at the local oscillator (LO) frequency. The transconductance stage of the mixer is working in analog mode, which is biased in saturation region. Under such mixed operation condition, the mixer circuit usually uses feature size devices due to the high frequency and high speed constrains. As a result, mixer performance is very vulnerable to reliability issues of deep submicro CMOS technology. Moreover, normally as the second stage of wireless receiver, its linearity performance is the dominant factor of the whole system, and it need to have moderate gain to reduce the noise figure of the following stage. The impact of the reliability issue on the CMOS RF mixer needs to be clearly understood because the operation of RF circuit is very sensitive to parameter variation [1].

Low power supply voltage, such as 1.8 V for the 0.18um CMOS, is generally considered beneficial for the hot carrier and Oxide reliability. However, in order to improve current drive capability and maintain device integrity, low V_{dd} technology is usually accompanied by reduction in gate oxide thickness, channel length and junction depth. These all lead to an increase in the channel and oxide electric field, a low V_{dd} technology may have shorter lifetime than a 5V-technology [2]. Experiments than hard break down for thinner oxide and stressed at lower, more realistic voltages [3].

In this paper, the experimental evidence of hot carrier and soft oxide breakdown is presented first. Device parameters before and after stress are extracted. Based on the RF mixer circuit operation condition, a comprehensive discussion is performed of MOSFET reliability taking into account channel hot carrier stress and soft oxide break down. Circuit degradation, as a result of shifted device parameters, is analyzed using the traditional circuit analysis techniques. Finally, mixer circuit redesign strategies is proposed to reduce alleviate the stress level.

II. EXPERIMENTAL DETAILS

The devices used in this work are 0.18 μm technology nMOSFETs. The gate width is 13.5 μm. the gate oxide thickness is 2.8 nm, stripped off 4.8 nm thick oxide growth. Massive transistors on the wafers are tested at room temperature to validate the statistical variance. The wafer is probed with the Cascade 12000 probe station and the Agilent 4156B precision semiconductor parameter analyzer. By means of voltage ramps, the hard breakdown voltage is determined to be -6 V for the accumulation

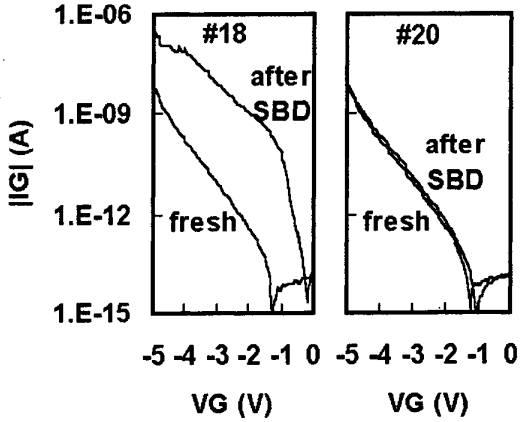

Fig. 1. I_G-V_G characteristics for the fresh and post-SBD devices. They shift upwards due to the stress induced leakage current (SILC)

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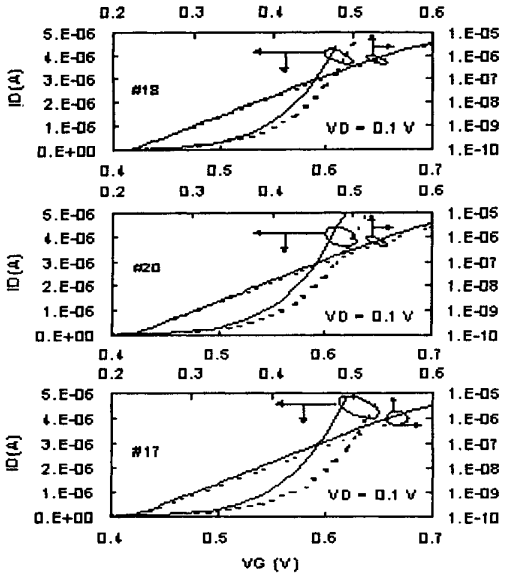

Fig. 2. I_D-V_G and logI_D-V_G showing shifts of V_t, g_m, and subthreshold current swing after SBD and HBD. The right hand side axis of I_D is in log scale.

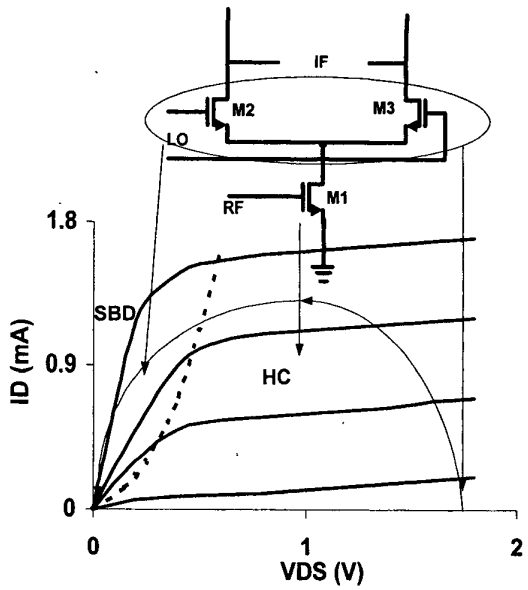

Fig. 3 Mixed operation point of mixer and related stress

mode stress with the source and drain either floated or grounded. It is +5.7 V for the inversion mode stress with the source and drain grounded. It is worth mentioning that if the source and drain are left floated in the inversion mode stress, the breakdown voltage is as large as 10 V.

The I_G-V_G characteristics for the fresh and post-stress devices are shown in Fig. 1. Due to the stress induced leakage current (SILC), all the *I-V* curves shift upwards. The threshold voltage, 0.54 V in average for the fresh devices, increases by about 3% after SBD, though the percentage is not as large as that after HBD, about 5%. The threshold voltage shift can be easily identified from Fig. 2. This figure also reveals the decrease of transconductance (the slope of the linear part of I_D-V_G curves in the figure) and the increase of sub-threshold current swing (the slope of the linear part of V_G-logI_D curves) after both SBD and HBD. In spite of the small decline of the early voltage (1%), the mobility is degraded up to 10 % after SBD, compared to 18% after HBD, extracted from the I_D-V_D families [4].

III. Degradation Under Mixed Circuit Operation Condition of RF Mixer

Since the maximum hot-carrier damage has traditionally been associated with the peak I_b region –approximately $V_{gs}=V_{ds}/2$ – and has been shown to be due to the creation of interface states [5], and the substrate current is exponentially proportional to $V_{ds} - V_{dsat}$. In Fig. 3, Mixer analog and digital operation condition is identified in the typical MOSFET output characteristic diagram. Gilbert Mixer is a half-analog half-digital circuit. The operation of mixer covers the entire region from cut-off, saturation to triode. A detailed CMOS mixer circuit with common mode feed back and power down switches is shown in Fig. 4.

In the mixer active mode, the transconductance (g_m) stage transistors M1 and M2 are usually operated with V_{dsat} of 200mV and V_{ds} of 550 mV in saturation region, as indicated in the central area in Fig. 3. The g_m stage transistor has double the drain current compared with that of the current switching stage. The depends on the level

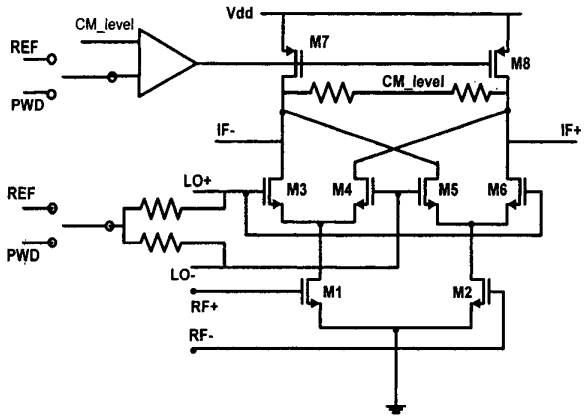

Fig. 4 CMOS Gilbert mixer with CMFB and power down mode

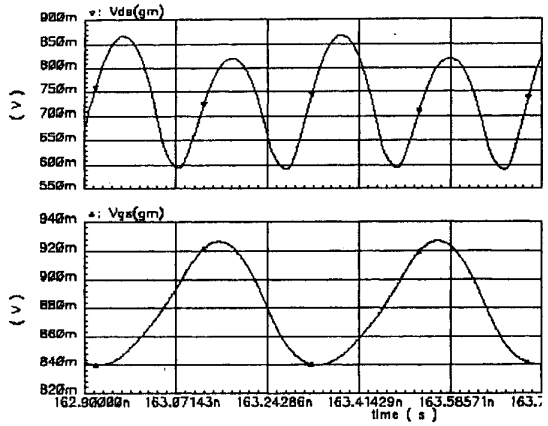

Fig. 5 V_{gs} and V_{ds} wave form of Gm stage (active mode)

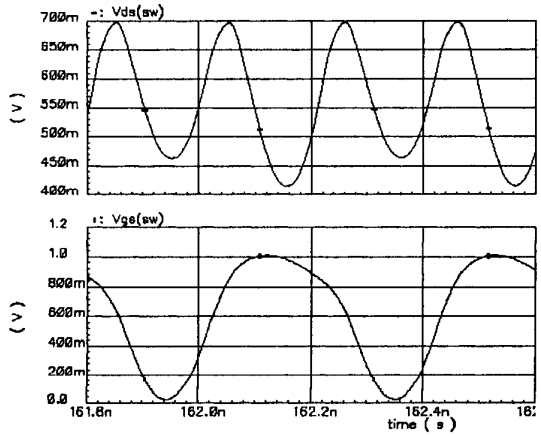

Fig. 6 V_{gs}, V_{ds} waveform of current switch stage (active mode)

of input signal, there exists substantial channel hot carrier stress in the I-V converter transistors because of high I_d and high V_{ds}. Fig. 5 shows the V_{gs} and V_{ds} waveform of g_m stage in mixer active mode. In some period of time, the V_{gs} could be close to $1/2V_{ds}$, which is the potential condition for maximum I_{sub}.

Since hot carrier only occurs when the transistor is in saturation region, which in the switch stage, occurs only during the transistor is in on state while V_{gs} is greater than V_t and V_{ds} is greater than V_{dsat}. Transistor will be in saturation when the switching curve travels form "off" to "on", as indicated in Fig.3. Unlike normal CMOS digital circuit, the "on " state of the mixer switch is closer to the saturation region than to the triode region. Fig. 6 shows V_{gs} and V_{ds} waveform of current switch stage. When V_{gs} is greater than the V_t (625 mV), V_{ds}, changing from 430mV to 700mV, is large enough to cause hot carrier. Moreover, degradation also depends on the LO frequency of the mixer. The higher the LO frequency is, the more damage the transistor experiences.

In order to have longer battery life, mixer circuit has a power down mode for portable application. In this mode, biasing voltage is switched off in order to avoid power consumption of the inactive circuit, but power supply voltages are not driven down in order to allow for fast reactivation of the circuit. In this mode, transistors are operating in subthreshold region, very small current and V_{ds}. So that these devices are not subjected to hot carrier stress. But high V_g can cause soft breakdown and possible high temperature cause V_t drift on M7 and M8 due to NBTI [6].

IV. CIRCUIT PERFORMANCE DEGRADATION MODELS

From the experiment in part II, two major device parameters, degraded by the HC and SBD effect, are threshold voltage (V_t) and mobility (μ). By treating HC and SBD degradation as perturbations to normal device parameters [7], the impact of degradation on mixer circuit performance can be treated as partial derivatives with respect to V_t and μ. Circuit performance degradation as a result of shifted device level parameters, can then be analyzed using traditional circuit analysis techniques.

Assuming a square-law MOSFET device, the conversion gain of Gilbert cell mixer can be approximated by averaging the gain over one period of LO signal [8].

$$A_v \approx g_m R_L \left(\frac{2}{\pi}\right)\left(1-\frac{\sqrt{2}(V_{gs}-V_t)_{sw}}{\pi V_{LO}}\right) \qquad (1)$$

With respect to V_T and μ, the mixer conversion gain degradation can be derived as

$$\frac{\Delta A_V}{A_V}=\frac{\Delta\mu}{\mu}+\frac{\left(-2+\frac{3\sqrt{2}(V_{gs}-V_t)}{\pi V_{LO}}\right)\Delta V_t}{(V_{gs}-V_t)\left(1+\frac{\sqrt{2}(V_{gs}-V_t)}{\pi V_{LO}}\right)} \qquad (2)$$

The distortion performance of the mixer was assumed to be limited by the input differential pair. With this assumption, the third order intermodulation intercept point (P_{IIP3}) for Gilbert cell can be approximated by performing a power series expansion on the input transconductance transfer function [9].

$$P_{IIP3}\approx\frac{8}{3}\frac{v_{sat}L}{\mu_1 R_s}V_{od}\left(1+\frac{\mu_1 V_{od}}{4v_{sat}L}\right)\left(1+\frac{\mu_1 V_{od}}{2v_{sat}L}\right)^2 \qquad (3)$$

Where $\mu_1=\mu_0+2\theta v_{sat}L$, and $V_{od}=V_{gs}-V_t$

Taking the silmilar approach, the effects of HC and SBD induced degradation of IIP3 is

$$\frac{\Delta P_{IIP3}}{P_{IIP3}} = -\frac{\left(\frac{1}{V_{gs}-V_t}+\frac{5\mu_1}{2v_{sat}L}+\frac{3\mu^2 V_{od}}{2(v_{sat}L)^2}+\frac{\mu^3 V_{od}^2}{4(v_{sat}L)^3}\right)}{\left(1+\frac{\mu V_{od}}{4v_{sat}L}\right)\left(1+\frac{\mu V_{od}}{2v_{sat}L}\right)^2}\Delta V_t + \frac{\left(-\frac{v_{sat}L}{\mu_1}+\frac{\mu V_{od}^2}{2v_{sat}L}+\frac{\mu^2 V_{od}^3}{8(v_{sat}L)^2}\right)}{\left(1+\frac{\mu V_{od}}{4v_{sat}L}\right)\left(1+\frac{\mu V_{od}}{2v_{sat}L}\right)^2}\Delta\mu_1 \quad (4)$$

V. CIRCUIT SIMULATION AND REDESIGN

As mentioned above, the factors that influence HC and SBD degradation in a transistor include its duration a transistor stay in the saturation region, its operation mode and transistor size, and the level of HC stress is proportional to V_{ds}-V_{dsat} and drain current I_d. Based these factors, a mixer circuit redesign strategies is described.

In order to reduce the damage in the current commuting switches, current injection could be added to the switching stage, as shown in Fig. 7. By adding two PMOS current source, the common mode current I_d through the switches reduce by 100uA each, and oxide stress is reduced because of smaller V_{gs}. Moreover the flicker noise of mixer is reduced because of more complete switching behavior without degrading the conversion gain and linearity property. The carefully biased cascode devices in the g_m stage reduce the V_{ds} and improve the LO-RF isolation. Biasing and sizing guideline from part IV to minimize the IIP3 and gain degradation are used. The improvement is summarized in Table I

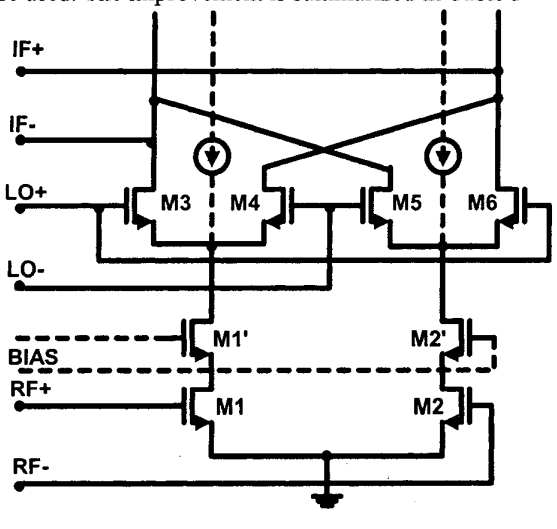

Fig. 7. Mixer circuit Reliability by Design

TABLE I
STRESS REDUCTION AFTER REDESIGN

	Id(SW) (mA)	*Vgs(SW) (mV)*	*Vds-Vdsat(gm) (mV)*
Stress Reduction	25%	3%	75%
Stress Type	HC	SBD	HC

VI. CONCLUSION

RF mixer is very vulnerable to hot carrier degradation. Soft breakdown happens more frequently than hard breakdown in lower power application. HC and SBD were characterized by monitoring major device parameter (V_t and μ) degradation. Circuit performance degradation was modeled by tracking device parameter variation. Mixer stress condition analysis was carried out under different operation condition. The redesign strategies show improved reliability with the same circuit performance.

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